



Sheet 1 of 1

Substitute Form PTO-1449 (Modified)		U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. <b>10559-310US1</b>	Application No. <b>10/070,091</b>
<b>Information Disclosure Statement</b> <b>by Applicant</b> <small>(Use several sheets if necessary)</small> <small>(37 CFR §1.98(b))</small>		Applicant <b>Gilbert Wolrich et al.</b>		
		Filing Date <b>February 27, 2002</b>	Group Art Unit	

<b>U.S. Patent Documents</b>							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
<i>g</i>	AA	09/473,571	12/28/1999	Wolrich et al.			
<i>g</i>	AB	09/475,614	12/30/1999	Wolrich et al.			
	AC						
	AD						
	AE						
	AF						
	AG						

<b>Foreign Patent Documents or Published Foreign Patent Applications</b>							
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes      No
<i>g</i>	AH	WO 01/16697	03/2001	WIPO			
<i>g</i>	AI	WO 01/16698	03/2001	WIPO			
<i>g</i>	AJ	WO 01/16703	03/2001	WIPO			
<i>g</i>	AK	WO 01/16713	03/2001	WIPO			
<i>g</i>	AL	WO 01/16714	03/2001	WIPO			
<i>g</i>	AM	WO 01/16715	03/2001	WIPO			
<i>g</i>	AN	WO 01/16716	03/2001	WIPO			
<i>g</i>	AO	WO 01/16722	03/2001	WIPO			
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<i>g</i>	AQ	WO 01/18646	03/2001	WIPO			
	AR						

<b>Other Documents (include Author, Title, Date, and Place of Publication)</b>		
Examiner Initial	Desig. ID	Document
<i>g</i>	AS	Paver et al., "Register Locking in Asynchronous Processor Computer Design: VLSI Processors," ICCD '92 Proceedings, IEEE 1992 International Conference, 1992, pp. 351-355.
<i>g</i>	AT	Waldspurger et al., "Register Relocation: Flexible Contents for Multithreading," Proceedings of the 20th Annual International Symposium on Computer Architecture," 1993, pp. 120-130.
	AU	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18  
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O P E R A T I O N  
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P A T E N T L I C E N S E M A R K O F F I C E U S C

## Title of Invention

## REGISTER SET USED IN MULTITHREADED PARALLEL PROCESSOR ARCHITECTURE

Application Number: 10/070091



Confirmation Number: 7309

First Named Applicant: Gilbert Wolrich

Attorney Docket Number: 10559-310US1

Search string: ( 3373408 or 3478322 or 3792441 or 3913074 or 3940745 or 4130890 or 4392758 or 4400770 or 4514807 or 4523272 or 4724521 or 4745544 or 4777587 or 4866664 or 5073864 or 5140685 or 5142683 or 5155831 or 5155854 or 5168555 or 5173897 or 5255239 or 5263169 or 5347648 or 5357617 or 5367678 or 5390329 or 5392391 or 5392411 or 5392412 or 5404464 or 5404482 or 5428809 or 5432918 or 5442756 or 5448702 or 5450351 or 5452437 or 5459842 or 5463625 or 5467452 or 5481683 or 5487159 or 5517628 or 5517648 or 5542070 or 5542088 or 5544236 or 5550816 or 5557766 or 20020053017 or 20020056037 or 20030041228 or 20030145159 or 20030191866 or 20040039895 or 20040054880 or 20040071152 or 20040073728 or 20040073778 or 20040098496 or 20040109369 or 20040205747 ).pn.

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Note: Applicant is not required to submit a paper copy of cited US Patent Documents

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h	2	3478322	1969-11-11	Evans			
h	3	3792441	1974-02-12	Wymore et al.			
h	4	3913074	1975-10-14	Homberg et al.			
h	5	3940745	1976-02-24	Sajeva			
h	6	4130890	1978-12-19	Adam			
g	7	4392758	1983-07-12	Bowles et al.			
h	8	4400770	1983-08-23	Chan et al.			
h	9	4514807	1985-04-30	Nogi			
h	10	4523272	1985-06-11	Fukunaga et al.			
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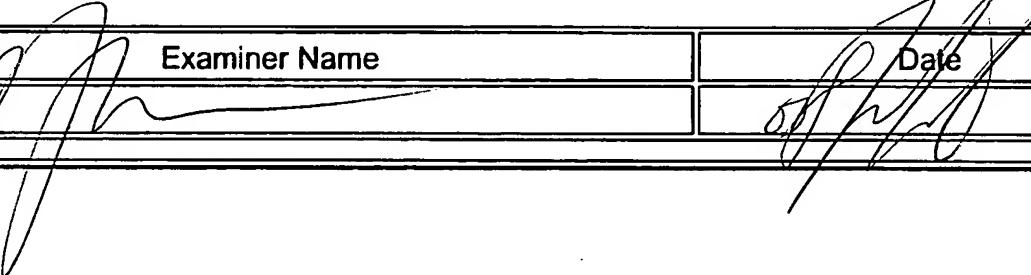
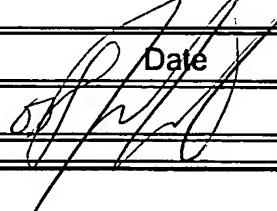
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Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
W	1	20020053017	2002-05-02	Adiletta et al.			
W	2	20020056037	2002-05-09	Wolrich et al.			
W	3	20030041228	2003-02-27	Rosenbluth et al.			
W	4	20030145159	2003-07-31	Adiletta et al.			
W	5	20030191866	2003-10-09	Wolrich et al.			
W	6	20040039895	2004-02-26	Wolrich et al.			
W	7	20040054880	2004-03-18	Bernstein et al.			
W	8	20040071152	2004-04-15	Wolrich et al.			
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W	11	20040098496	2004-05-20	Wolrich et al.			
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# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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## Title of Invention

## REGISTER SET USED IN MULTITHREADED PARALLEL PROCESSOR ARCHITECTURE

Application Number: 10/070091



Confirmation Number: 7309

First Named Applicant: Gilbert Wolrich

Attorney Docket Number: 10559-310US1

Search string: ( 5568617 or 5574922 or 5574939 or 5592622 or 5606676 or 5613071 or 5613136 or 5623489 or 5627829 or 5630130 or 5644623 or 5649157 or 5659722 or 5680641 or 5689566 or 5692167 or 5699537 or 5717898 or 5721870 or 5742587 or 5742782 or 5742822 or 5745913 or 5751987 or 5761507 or 5761522 or 5781774 or 5784649 or 5784712 or 5796413 or 5797043 or 5809235 or 5809530 or 5812839 or 5812868 or 5828746 or 5828863 or 5832215 or 5835755 or 5854922 or 5860158 or 5886992 or 5887134 or 5890208 or 5892979 or 5905876 or 5905889 or 5915123 or 5933627 or 5659687 ).pn.

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Note: Applicant is not required to submit a paper copy of cited US Patent Documents

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2	2	5574922	1996-11-12	James			
3	3	5574939	1996-11-12	Keckler et al.			
4	4	5592622	1997-01-07	Istfeld et al.			
5	5	5606676	1997-02-25	Grochowski et al.			
6	6	5613071	1997-03-18	Rankin et al.			
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9	9	5627829	1997-05-06	Gleeson et al.			
10	10	5630130	1997-05-13	Perotto et al.			
11	11	5644623	1997-07-01	Gulledge			
12	12	5649157	1997-07-15	Williams			
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# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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## REGISTER SET USED IN MULTITHREADED PARALLEL PROCESSOR ARCHITECTURE

Title of Invention Application Number: 10/070091

Confirmation Number: 7309

First Named Applicant: Gilbert Wolrich

Attorney Docket Number: 10559-310US1

Search string: ( 5937187 or 5938736 or 5940612 or 5940866 or 5946487 or 5948081 or 5951679 or 5958031 or 5961628 or 5970013 or 5978838 or 5983274 or 5996068 or 6002881 or 6009515 or 6012151 or 6014729 or 6023742 or 6058168 or 6058465 or 6067585 or 6070231 or 6072781 or 6073215 or 6076158 or 6079008 or 6079014 or 6085215 or 6085294 or 6092127 or 6092158 or 6112016 or 6115811 or 6134665 or 6141689 or 6141765 or 6144669 or 6145054 or 6157955 or 6160562 or 6182177 or 6195676 or 6199133 or 6201807 or 6212542 or 6212611 or 6216220 or 6223207 or 6009505 or 6029228 ).pn.

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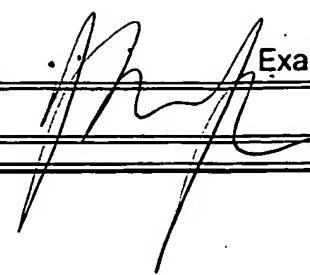
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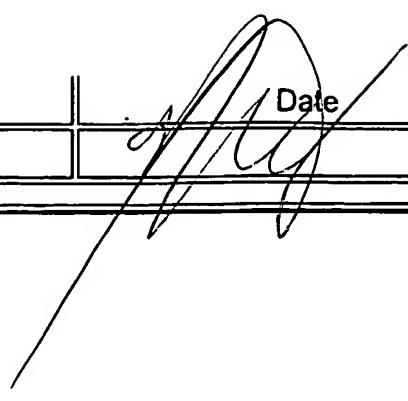
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l	2	5938736	1999-08-17	Muller et al.			
l	3	5940612	1999-08-17	Brady et al.			
g	4	5940866	1999-08-17	Chisholm et al.			
z	5	5946487	1999-08-31	Dangelo			
o	6	5948081	1999-09-07	Foster			
w	7	5951679	1999-09-14	Anderson et al.			
w	8	5958031	1999-09-28	Kim			
m	9	5961628	1999-10-05	Nguyen et al.			
f	10	5970013	1999-10-19	Fischer et al.			
v	11	5978838	1999-11-02	Mohamed et al.			
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h	13	5996068	1999-11-30	Dwyer III et al.			
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✓	17	6014729	2000-01-11	Lannan et al.
✓	18	6023742	2000-02-08	Ebeling et al.
✓	19	6058168	2000-05-02	Braband
✓	20	6058465	2000-05-02	Nguyen
✓	21	6067585	2000-05-23	Hoang
✓	22	6070231	2000-05-30	Ottinger
✓	23	6072781	2000-06-06	Feeney et al.
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✓	26	6079008	2000-06-20	Clery III
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✓	32	6112016	2000-08-29	MacWilliams et al.
✓	33	6115811	2000-09-05	Steele Jr.
✓	34	6134665	2000-10-17	Klein et al.
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✓	37	6144669	2000-11-07	Williams et al.
✓	38	6145054	2000-11-07	Mehrotra et al.
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✓	40	6160562	2000-12-12	Chin et al.
✓	41	6182177	2001-01-30	Harriman
✓	42	6195676	2001-02-27	Spix et al.
✓	43	6199133	2001-03-06	Schnell
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✓	45	6212542	2001-04-03	Kahle et al.
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Examiner Name

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## REGISTER SET USED IN MULTITHREADED PARALLEL PROCESSOR ARCHITECTURE

Title of Invention Application Number: 10/070091

Confirmation Number: 7309

First Named Applicant: Gilbert Wolrich

Attorney Docket Number: 10559-310US1

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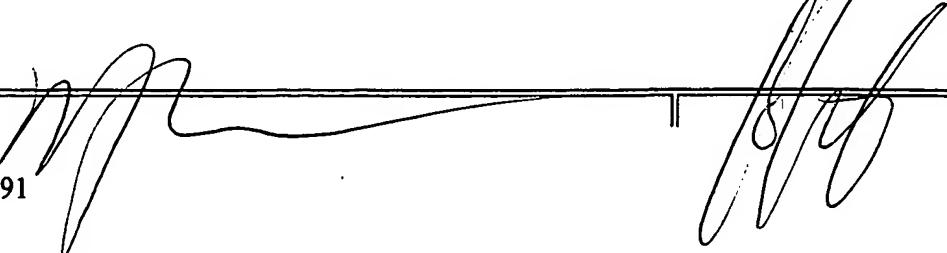
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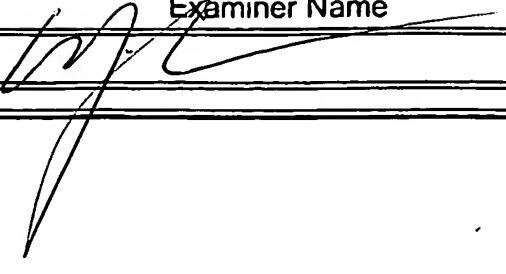
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1	1	6223238	2001-04-24	Meyer et al.			
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3	3	6247025	2001-06-12	Bacon			
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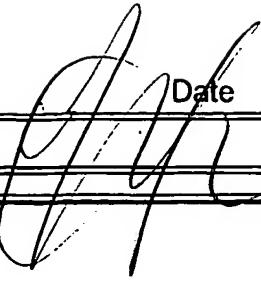
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30	6584522	2003-06-24	Wolrich et al.
31	6587906	2003-07-01	Wolrich et al.
32	6606704	2003-08-12	Adiletta et al.
33	6625654	2003-09-23	Wolrich et al.
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47	5652583	1997-07-29	Kang
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50	5450603	1995-09-12	Davies

Signature





Examiner Name



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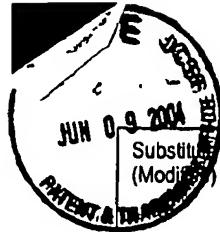
Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-310US1	Application No. <b>10/070091</b>
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)		Applicant Gilbert Wolrich et al.	
		Filing Date	Group Art Unit
(37 CFR §1.98(b))			

U.S. Patent Documents							
Examiner Initial	Desig. ID	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date If Appropriate
<i>AB</i>	AA	5,357,617	10/18/1994	Davis et al.			
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<i>HN</i>	AC	6,092,175	07/18/2000	Levy et al.			
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Other Documents (include Author, Title, Date, and Place of Publication)		
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	AT	

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Substitute Form PTO-1449 (Mod.)		U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-310US1	Application No. 10/070,091
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.		
		Filing Date February 27, 2002	Group Art Unit 2183	

Foreign Patent Documents or Published Foreign Patent Applications							
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes <input checked="" type="checkbox"/> No <input type="checkbox"/>
h	AA	WO 01/50679	07/12/2001	WIPO			
h	AB	WO 01/50247	07/12/2001	WIPO			
h	AC	WO 01/48619	07/05/2001	WIPO			
h	AD	WO 01/48606	07/05/2001	WIPO			
h	AE	WO 01/48599	07/05/2001	WIPO			
h	AF	WO 01/48596	07/05/2001	WIPO			JUN 10 2004
h	AG	WO 01/41530	06/14/2001	WIPO			Technology Center 2100
h	AH	WO 01/16782	03/08/2001	WIPO			
h	AI	WO 01/16770	03/08/2001	WIPO			
h	AJ	WO 01/16769	03/08/2001	WIPO			
h	AK	WO 01/16718	03/08/2001	WIPO			
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h	AM	WO 97/38372	10/16/1997	WIPO			
h	AN	WO 94/15287	07/07/1994	WIPO			
h	AO	EP 0 809 180	11/26/1997	Europe			
h	AP	EP 0 745 933	12/04/1996	Europe			
h	AQ	EP 0 633 678	01/11/1995	Europe			
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Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
h	AU	Agarneal et al., "April: A Processor ArchitectUre for Multiprocessing," Proceedings of the 17 <sup>th</sup> Annual International Symposium on Computer Architecutre, IEEE, pp. 104-114.
h	AV	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
h	AW	Chang et al., "A New Mechanism For Improving Branch Predictor Performance," IEEE, pp. 22-31 (1994).

Examiner Signature	Date Considered
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Sheet 2 of 2Substitute Form PTO-1449  
(Modified 10-2000)U.S. Department of Commerce  
Patent and Trademark OfficeAttorney's Docket No.  
10559-310US1Application No.  
10/070,001
**Information Disclosure Statement**  
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<b>Other Documents (include Author, Title, Date, and Place of Publication)</b>		
Examiner Initial	Desig. ID	Document
<i>W</i>	AX	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 <sup>nd</sup> ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.
<i>W</i>	AY	Farkas et al., "The multicluster architecture: reducing cycle time through partitioning," IEEE, vol. 30, December 1997, pp. 149-159.
<i>W</i>	AZ	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
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<i>W</i>	ABB	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
<i>W</i>	ACC	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997.
<i>W</i>	ADD	Hennessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482.
<i>W</i>	AEE	Hyde, R., "Overview of Memory Management," <i>Byte</i> , vol. 13, no. 4, 1998, pp. 219-225.
<i>W</i>	AFF	Intel, "IA-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21.
<i>W</i>	AGG	Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998.
<i>W</i>	AHH	Litch et al., "StrongARMing Portable Communications," <i>IEEE Micro</i> , 1998, pp. 48-55.
<i>W</i>	AII	Mendelson et al., "Design Alternatives of Multithreaded Architecture," <i>International Journal of Parallel Programming</i> , vol. 27, no. 3, Plenum Press, New York, USA, June 1999, pp. 161-193.
<i>W</i>	AJJ	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, <i>Online!</i> , 13 November 1998.
<i>W</i>	AKK	Thistleton et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
<i>W</i>	ALL	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28 <sup>th</sup> Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
<i>W</i>	AMM	Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1998.
<i>W</i>	ANN	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online</i> , 18 March 1999.
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<i>W</i>	APP	Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7.
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